REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-42 in the application. The Examiner has indicated that Claims 21-42 are allowable and that Claims 9 and 19 would be allowable if rewritten in independent form. (*See* Examiner's Action, page 4.)

In a prior response, the Applicants amended Claims 1-7, 9-11, 21 and 31 and canceled Claims 8 and 18. In the present response, no claims have been canceled, added or amended. Accordingly, Claims 1-7, 9-17 and 19-42 are currently pending in the application. Additionally, the Applicants assert that all of the pending claims are allowable.

I. Rejection of Claims 1-7, 10-17 and 20 under 35 U.S.C. § 102

The Examiner has rejected Claims 1-7, 10-17 and 20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,347,347 B1 to Brown, *et al.* The Applicants respectfully traverse the rejection, because Brown does not teach each and every element of independent Claims 1 and 11.

Brown is directed to a data transfer technique that employs direct memory access (DMA) logic to transfer data to a memory and simultaneously store the data into a buffer that is closely coupled to a processor. *See* Abstract. Brown teaches a network interface card (NIC) 10 comprising an application-specific integrated circuit (ASIC) 16, which in turn comprises a processor 28. *See* column 2, line 63 to column 3, line 14. The Examiner cites Brown at column 4, lines 36-47 and Figures 1 and 2 to assert that Brown anticipates the element of Claims 1 and 11, "a programmable logic core having an array of dynamically configurable arithmetic logic units." *See* Examiner's Response ¶ 3. The Applicants respectfully disagree.

Instead, Brown teaches:

> FIG. 2 shows the processor 28 in more detail. The processor core 30 interfaces with the instruction RAM 32 via an instruction address (IA) bus 60 and an instruction data (ID) bus 62. Also, the processor core 30 interfaces with the data RAM 34 via a data address (DA) bus 64 and a data data (DD) bus 66. The DD bus 66 is connected as a data input to the instruction RAM 32, and a multiplexer 68 is used to select either the IA bus 60 or the DA bus 64 as the source of the address to the instruction RAM 32. This configuration enables the processor core 30 to load operational code into the instruction RAM 32 by performing data store operations into an appropriate address space.

Column 4, lines 36-47. This passage cited by the Examiner teaches various elements of the processor 28, including a RAM 34, multiplexer 68, and several communication buses. However, there is no teaching of a *single* arithmetic logic unit (ALU), much less *an array* of dynamically configurable ALUs. Moreover, one skilled in the art understands that the various elements present in Brown's processor are not equivalent to an ALU.

Therefore, Brown does not anticipate the element "a programmable logic core having an array of dynamically configurable arithmetic logic units," and does not defeat the novelty of independent Claims 1 and 11. Thus, Claims 1 and 11, and those claims depending therefrom, are allowable. Accordingly, the Applicants respectfully request that the Examiner withdraw the rejection of Claims 1-7, 10-17 and 20 under 35 U.S.C. § 102(e) and allow issuance thereof.

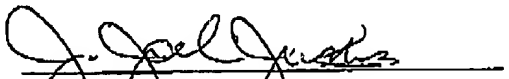
II. Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-7, 9-17, and 19-42.

The undersigned does not believe that any fees are due regarding this matter. However, he does hereby authorize the Commissioner to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395. The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES, PC



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